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Low-power and high-performance 1-bit set Full-adder

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Abstract

An adder is an important element of all the arithmetic and logic units. The recent trend in Nanotechnology is moving towards the need of the devices, which consume low power. The Single Electron Transistor (SET), distinguished by a very small device size low power dissipation, high speed and high performance, is one of the most promising nano electronics devices to replace conventional CMOS. The SET technology offers the ability to control the motion of individual electrons in the designed circuits. In this Full Adder Circuit we were used 24 SET and 14 resistors. The circuit is functioning as required for all the combination of input voltage. This work evaluates the performance of the proposed designs in terms of delay, area, power, and their products by hand with logical effort and through custom design and layout in SET process technology. Also shown is the considerable impact of the supply-voltage scaling on reducing the power expended by leakage and short-circuit. The Low-Power and High-Performance 1-Bit Set Full-Adder digital circuits have been simulated by PSPICE 9.1.

Keywords: SET, Full Adder, High-Speed.
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1. Introduction

The performance of many applications such as digital signal processing depends on the performance of the arithmetic circuits to execute complex algorithms such as convolution, correlation and digital filtering. Usually, the performance of the integrated circuits is influenced by how the arithmetic operators are implemented in the cell library provided to the designer and used for synthesizing. As more complex arithmetic circuits are presented each day, the power consumption becomes more important.

The arithmetic circuits grows more complex with the increasing processor bus width, so energy consumption is becoming more important now than ever due to the increase in the number and density of transistors on a chip and faster clock Increasing demand for fast growing technologies in mobile electronic devices such as cellular phones, PDA's and laptop computers Requires the use of a Single Electron Transistor Full Adder in Nano Technology systems since it is the core element of arithmetic circuits. Decreasing the power supply leads to power consumption reduction.

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Single electron transistor (SET) is a new type of switching device that uses controlled electron tunneling to amplify current. SET is distinguished by a very small device size and ultra-low power dissipation and based on controlling the transport of an individual electron. In 1987, Likharev has proposed a single-electron transistor in which the tunneling of the electrons is controlled by a bias applied at the center electrode [1]. Since then, various solutions have been developed on logic circuits, memory and other circuits. The first single electron inverter, made from two complementary SETs was proposed by Tucker et al. in 1992 [2]. This work explained the principles of designing complementary SETs, that corresponds to the PMOS and NMOS transistors, which can be used to design CMOS-style logic.

2. Basic Physics of SET Operation

Single Electron Transistor [SET] has been made with critical dimensions of just a few nanometer using metal, semiconductor, carbon nanotubes or individual molecules. A SET consists of a small conducting island [Quantum Dot] coupled to source and drain leads by tunnel junctions and capactively coupled to one or more gate. Unlike Field Effect transistor, Single electron device based on an intrinsically quantum phenomenon, the tunnel effect. The electrical behaviour of the tunnel junction depends on how effectively barrier transmit the electron wave, which decrease exponentially with the thickness and on the number of electron waves modes that impinge on the barrier, which is given by the area of tunnel junction divided by the square of wave length.

3. Quantum Dot [Qd]

Quantum dot [QD] is a mesoscopic system in which the addition or removal of a single electron can cause a change in the electrostatic energy or Coulomb energy that is greater than the thermal energy and can control the electron transport into and out of the QD. This sensitivity to individual electrons has led to electronics based on single electrons. For QD, the discrete energy level of the electrons in the QD becomes pronounced, like those in atoms and molecules, so one can talk about “artificial atoms and molecules”. When the wave functions between two quantum dots overlap, the coupled quantum dots exhibit the properties of a molecule. To understand the electron transport properties in QD. Let us consider a metal nanoparticle sandwiched between two metal electrodes shown in Fig. 1. The nanoparticle is separated from the electrodes by vacuum or insulation layer such as oxide or organic molecules so that only tunneling is allowed between them. So we can model each of the nanoparticles-electrode junctions with a resistor in parallel with a capacitor. The resistance is determined by the electron tunneling and the capacitance depends on the size of the particle. We denote the resistors and capacitors by R1, R2, C1 and C2, and the applied voltage between the electrodes by V. We will discuss how the current, I depends on V. When we start to increase V from zero, no current can flow between the electrodes because movement of an electron onto (charging) or off (discharging) from an initially neutral nanoparticle cost energy by an amount given by equation 1.

$$E = {}^{e^2}/_{2C} \tag{1}$$

This suppression of electron flow is called Coulomb blockade. Current start to flow through the nanoparticles only when the applied voltage V is large enough to establish a voltage φ at the nanoparticles such that

$$e\varphi \geq E = \frac{e^2}{2C} \tag{2}$$

This voltage is called threshold voltage and denoted by Vth. So in the I-V curve, we expect a flat zero-current regime with a width of 2 Vth. When the applied voltage reaches Vth, an electron is added to (removed from) the nanoparticles. Further increasing the voltage, the current does not increase proportionally because it requires us to add (or remove) two electrons onto the nanoparticles, which cost a greater amount of energy. Once the applied voltage is large enough to overcome the Coulomb energy of two electrons, the current starts to increase again. This leads to a stepwise increase in I-V curve, called Coulomb staircase.

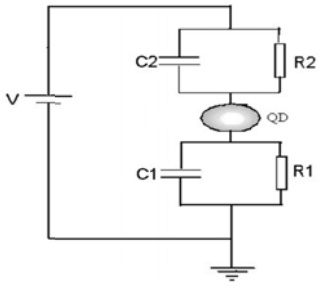

Fig. 1: Quantum Dot Structure.

4. Single Electron Tunneling

The principals of single-electron electronics have been presented in many publications [6, 7]. Summarizing, in the single-electron technology, the circuits consist of conducting islands, tunnel junctions, capacitors, and voltage sources. The islands are arbitrarily connected with tunnel junctions, capacitors and voltage sources. The basic component of single electron tunneling technology is the tunnel junction. A tunnel junction can be considered as two conductors separated by a thin layer of insulating material. A tunnel junction and its schematic diagram are shown in Fig. 2. It is characterized by a capacitance Cj and a resistance R_j, each of which depends on the physical size of the tunnel junction and the thickness of the insulator. The fundamental principle of SET devices and circuits is the Coulomb blockade [5].

5. Structure of Single-Electron Transistors

Single-electron transistors (SETs) are three-terminal switching devices, which can transfer electrons form source to drain one by one. The schematic structure of SETs is shown in Fig. 1. A SET is made from two tunnel junctions that share a common electrode. A tunnel junction consists of two pieces of metal separated by a very thin insulator. The only way for electrons in one of the metal electrodes to travel to the other electrode is to tunnel through the insulator. Since tunneling is a discrete process, the electric charge that flows through the tunnel junction flows in multiples of e, the charge of a single electron [3]. Here we have three terminal Source, Drain and Gate. As shown in the figure, the structure of

SETs is almost the same as that of MOSFETs. However, SETs have tunneling junctions in place of pn-junctions of the MOSFETs and a quantum dot in place of the channel region of the MOSFETs [1, 8].

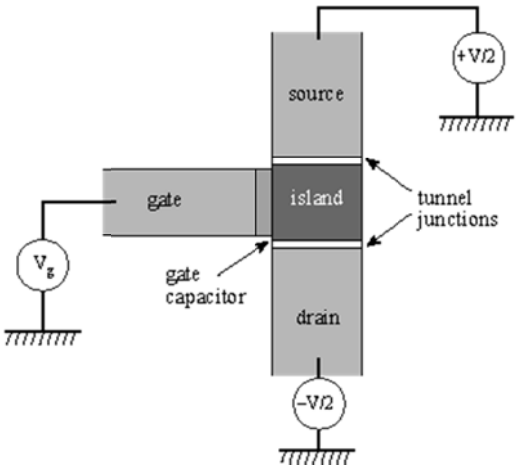

Fig. 2: Schematic structure of SET.

6. Low-Power and High-Performance 1-Bit SET Full-Adder

In general, there are three components that constitute the amount of power consumed in circuit operation: dynamic, short-circuit, and leakage power. The dynamic power is consumed due to the charging and discharging of the output capacitance CL when logic switching occurs, and thus, is inevitable in circuit operation. Short-circuit power occurs when both the NSET and PSET are turned-on simultaneously, conducting short-circuit current from the supply to the ground. The power resulting from the short-circuit current is only a minor fraction of the total dissipation, as long as the output transient times are relatively large compared to the input rise and fall times. However, the short-circuit power in SET circuits is also a function of operation temperature, and, as the temperature increases, it make up a considerable portion of the total power.

The most significant component of the power consumed in the SET circuit is the leakage power. An ideal complementary circuit does not dissipate power when the input does not change. However, in a circuit composed of SETs, leakage power is dissipated by the thermal enhancement of normal tunneling and co-tunneling. The static leakage power due to the thermal enhancement of normal tunneling makes up a considerable portion of the total power as the operation temperature increases.

Because the dynamic power has a quadratic dependence on the supply-voltage, and both the current level and voltage level rise as the dimensions of SETs are scaled down, supply voltage scalability, while device parameters remain constant, is a key factor in constructing low-power SET circuits.

The 1- Bit SET Full-adder is a basic arithmetic block which has three inputs (the addend A (1-bit precision), the augend B (1-bit precision), and the carry-in (C_i) and two outputs the sum S, and the carry-out C_o.

Fig. 3 shows an Internal Circuit of Low-Power and High-Performance 1-Bit SET Full-Adder circuit. It consist of 14 PSET and 14 NSET Transistor. The supply voltage V_{dd} is constant and its value is 25 mV. The voltage sources V_1, V_2 and V_3, shown in Fig. 2, are the inputs (A, B and C_{in} respectively) of the full-adder and it can take only two values 0.0 V which corresponds to the logic `0', and 25 mV which corresponds to the logic `1'. The input

voltage V1(A) is applied to PSET 1, 4, 7, 10 and NSET of 21, 18, 24, 26 through gate, input voltage V2(B) is applied to PSET 2, 3, 5, 14 and NSET of 17, 19, 20, 22 through gate, and the input voltage V3(C_{in}) is applied to PSET 6, 8, 13 and NSET of 15, 16, 28 through gate. The output signals of the full-adder sum is taken from source of PSET 9 and drain of NSET 27, and N6, and the Carry is taken from source of PSET 11 and drain of NSET 25. The presence of positive charge corresponds to logic `1', whereas no charge corresponds to logic `0'.

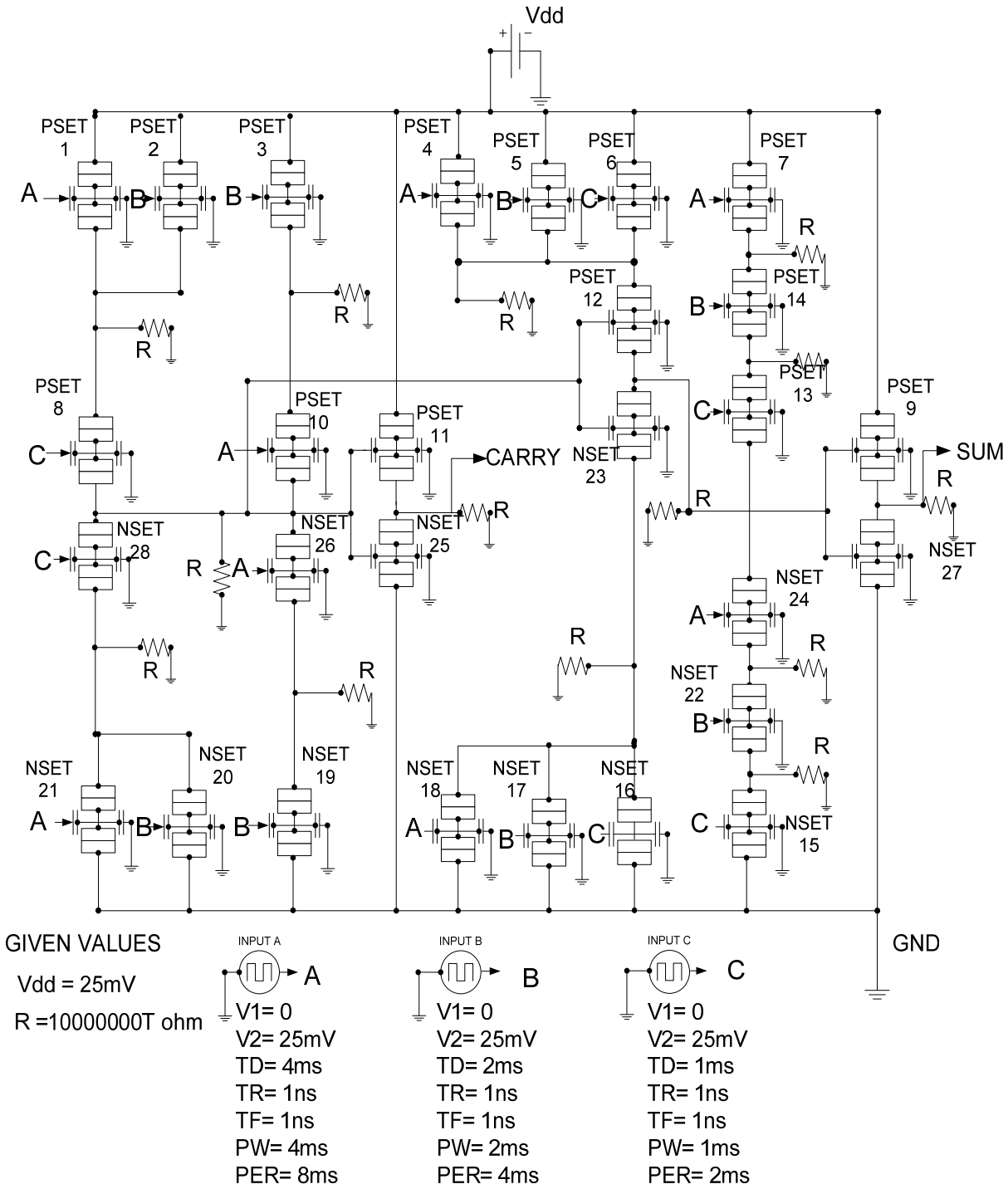

Fig. 3: Internal Circuit of Low-Power and High-Performance 1-Bit SET Full-Adder.

7. Simulation Results

The logic operation of the full-adder is shown in Fig. 4. In this first 3 rows show the time variation of the input V_1 and V_2, respectively. The piecewise constant and apply all possible combinations of logic '0' and '1' to the circuit. The remaining 2 rows are shows the output sum and carry respectively. When we applied input voltage [0 0 1] then we get sum is logic '1' and carry is logic '0'. When we applied input voltage [0 1 1] then we get sum is logic '0' and carry is logic '1'. When we applied input voltage [0 0 0] then we get the both sum and carry is logic '0'.

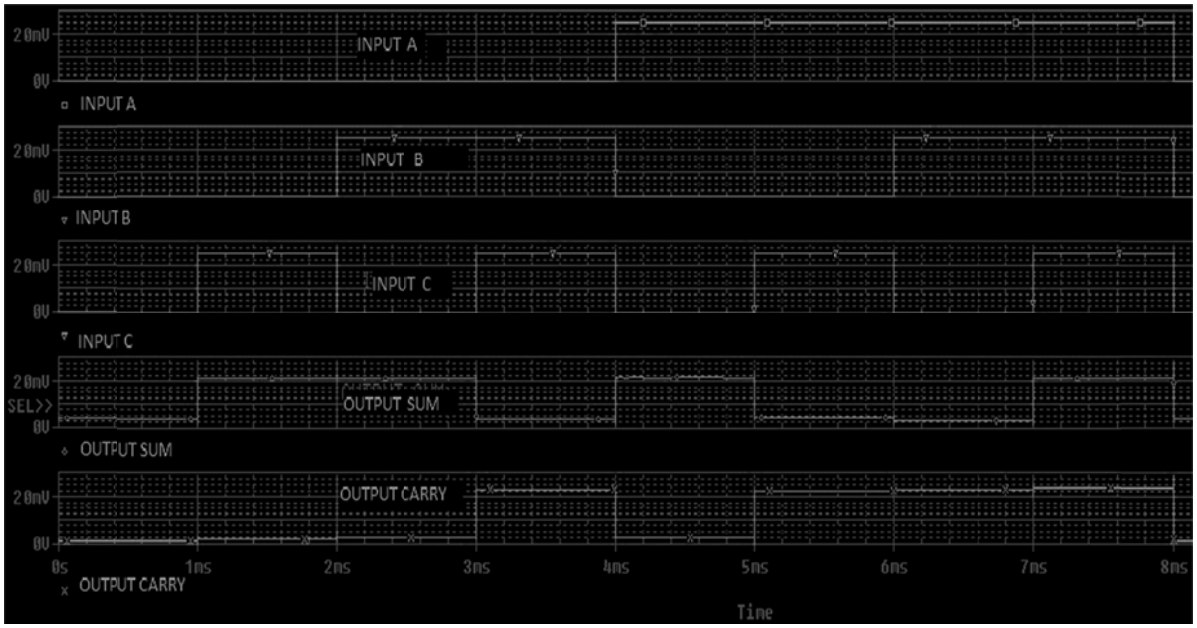

Fig. 4: Simulated input (A B C) and Simulated output (SUM & CARRY).

8. Conclusion

The Design considerations for Low-Power and High-Performance 1-Bit SET Full-Adder logic circuits have been investigated. It has also been shown that the supply-voltage scaling is an effective method for the reduction of power consumed by leakage and short-circuit. Simulation results reveal that the supply-voltage scaling should be carried out within 20% of V^{m}_{DD} to maintain overall circuit performance. Truth table is achieved for the operation of SET function based adder and the circuit is designed using PSPICE 9.1 Outputs are verified for the input set and the performance metrics of the efficient full adder are measured and tabulated. 1 bit SET full adder shows 55% reduction of power consumption. Area, and Delay are reduced than their conventional adders. As technology scaling is increased possibility for high reduction in power dissipation and area. So 1 bit SET full adder realizations can be considered as a best choice for the multipliers.

Future Work

Further this multiplier can be implemented in filters for image processing applications. Due to the increase in speed of multiplier and high reduction in power dissipation it can be used for DSP applications.

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